

FIG. 1A

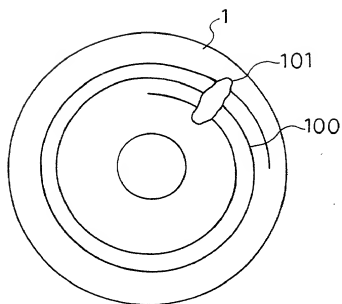
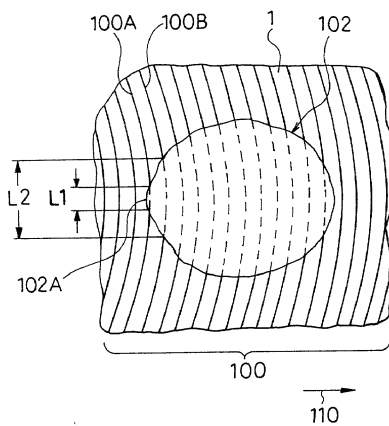


FIG. 1B



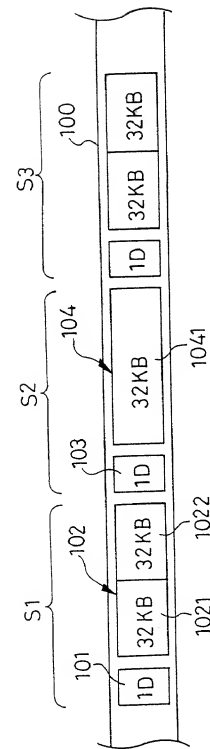


FIG. 2B

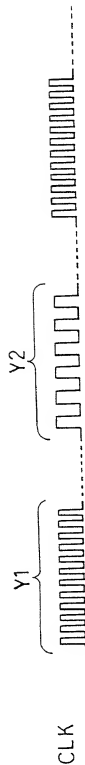


FIG. 2C

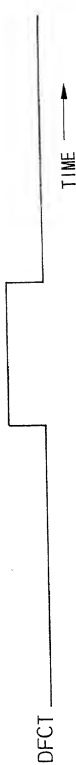


FIG. 4A

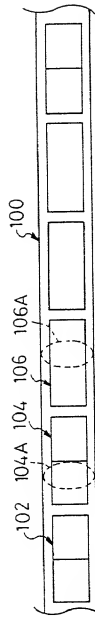


FIG. 4B
BLOCK SYNCHRONIZING
SIGNAL IDSNC

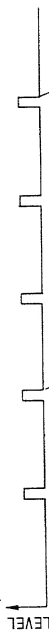


FIG. 4C OUTPUT SIGNAL RF

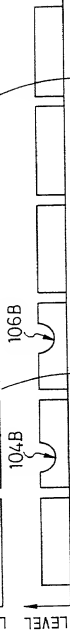
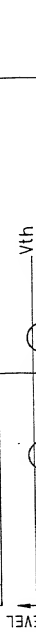
FIG. 4D
DECREMENT SIGNAL ΔA
OF OUTPUT SIGNAL RFFIG. 4E
SET PULSE DFSETFIG. 4F
RESET PULSE DFRST

FIG. 4G

DEFECT DETERMINATION
SIGNAL DFCT



FIG. 4H

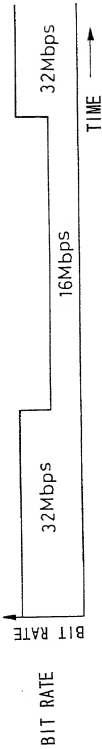


FIG. 5A

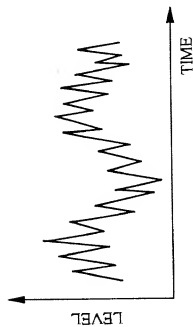


FIG. 5B

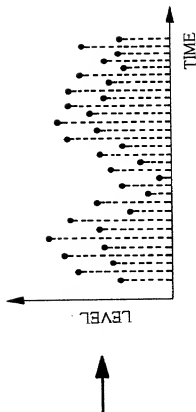


FIG. 5C

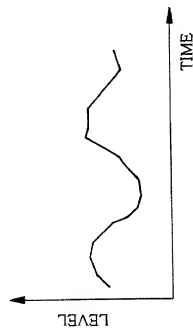


FIG. 5D

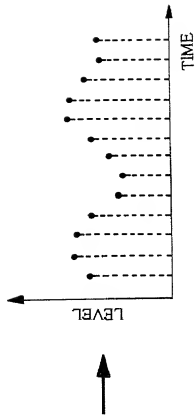


FIG. 6

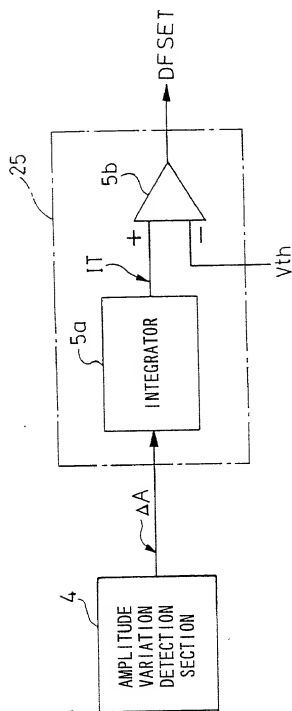
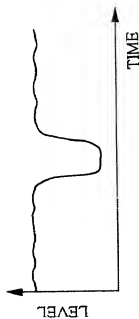


FIG. 7A RF1



RF2

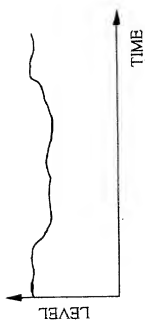


FIG. 7B AA1



AA2

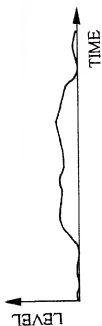
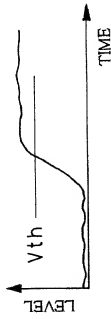


FIG. 7C IT1



IT2

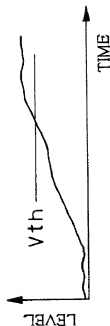
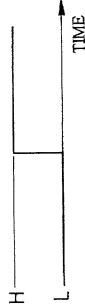
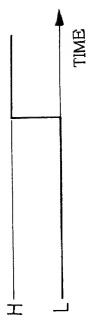


FIG. 7D DFSET



DFSET



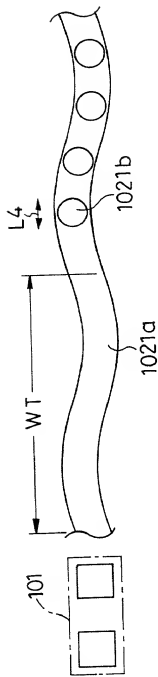


FIG. 8A

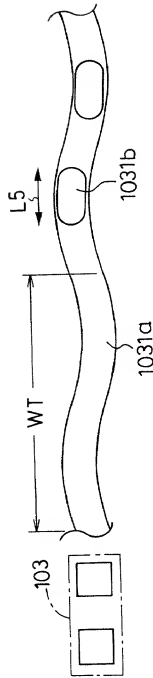


FIG. 8B